The Y Project

Worldwide
Information
Systems

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Bull

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Agenda

- Context of the project
- Genesis of the architecture
  - Architectural Principles
  - Capability Based Addressing
  - Address Space Management
  - Instruction Set Architecture
  - Hardware Architecture
- People
- Epilog

Context of the Project

- In parallel with the UNIDATA agreement (development of the X Line), launch by the end of 1972 at CII of a study group in charge of the definition of a new product line, dubbed Y Line, to be shipped in the early 80's
- Y Line aimed at the convergence of incompatible product lines. Rumors about IBM's FS project (discontinued compatibility with S/370)
- **Requirements**
  - **Protection and Security**
  - **Policy and Mechanism Separation**
  - **Minimizing complexity of the development of Operating Systems**
  - **Architecture Longevity**
  - **Software Portability**
  - **Symmetric Multiprocessor**
  - **Management of Very Large Data Sets**
- Launch of a common study group within UNIDATA in 1974

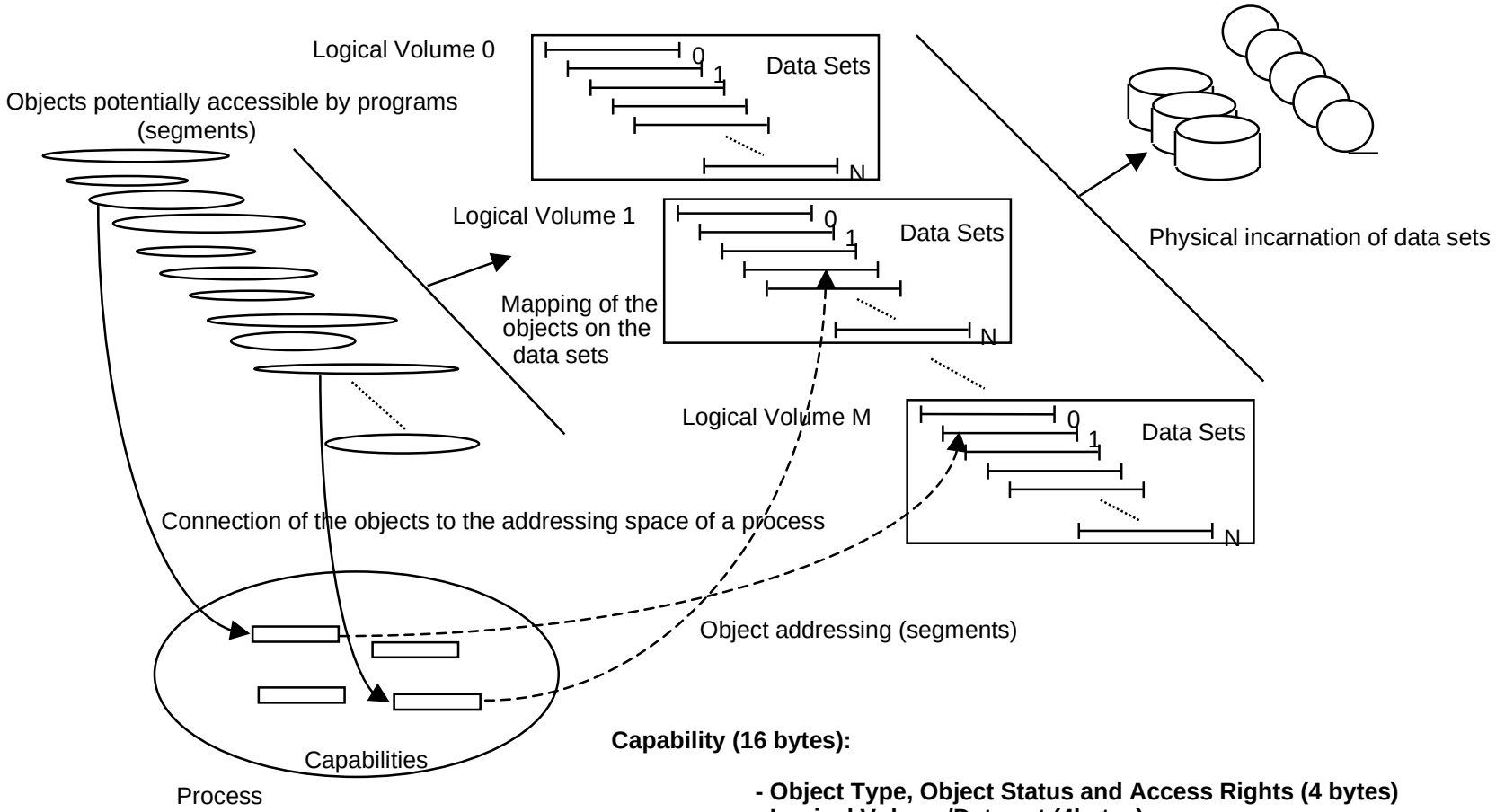
Genesis of the Architecture

- Choice between two approaches to relax the strict binary compatibility constraint:
  - Virtual Machine (i.e. CP/CMS)
  - Abstract Machine
- Virtual Machine no longer considered (perpetuation of the limitations of the base architecture)
- Abstract Machine selected - MULTICS was the first architectural model considered:
  - Unique Addressing Space (one level store): files mapped in the addressing space
  - Dynamic Linkage Editor
- Difficulties faced with this first approach:
  - Structuring the addressing space
  - Protection
- New approach then considered: capability-based architecture

Architectural Principles

- Unique Virtual Space and Single Level with 64 bits addresses
- Addressing Space structured as 2^{32} "data sets", of up to 2^{32} bytes each
- Concept of segment (window): unit of addressing and protection interpreted by the hardware but managed by the system software
- Symbolic naming of all objects, flexible organization of the name space (organization not defined up front)
- Capability-based addressing
- Partition principle (i.e. "tag" approach rejected, capabilities contained within specific segments)
- Two level architecture
  - Base Architecture (capability-based addressing)
  - Virtual Architecture (Instruction Set Architecture built on top of the base architecture)
- Object-oriented system software

Capability-based Addressing



Capability (16 bytes):

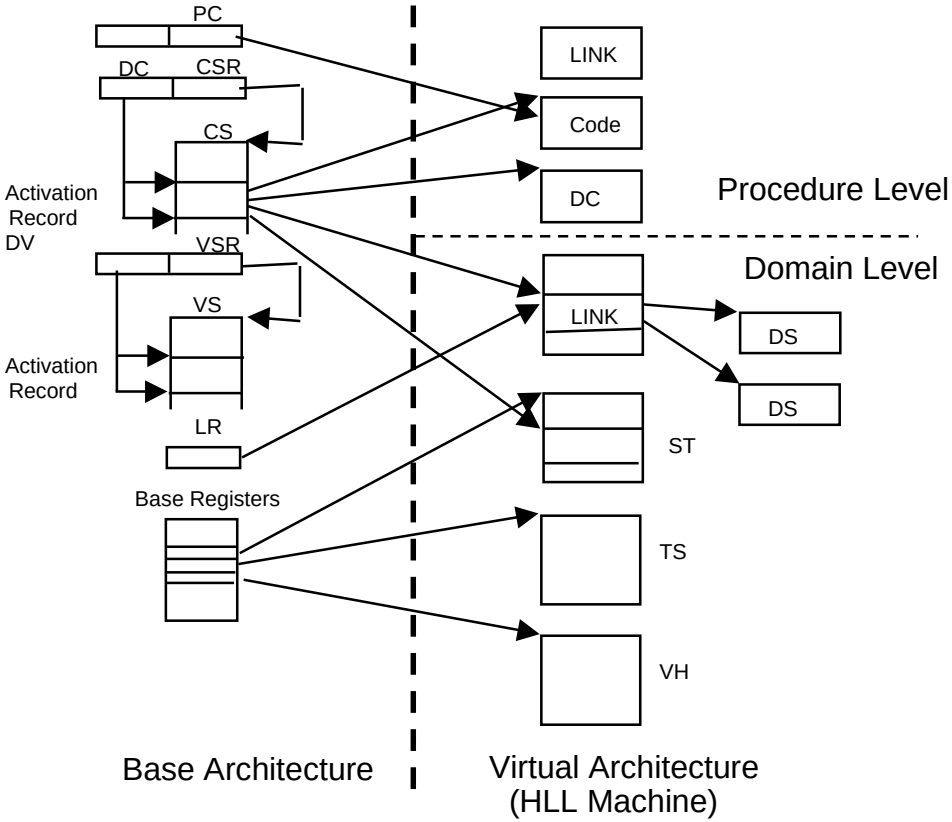
- **Object Type, Object Status and Access Rights (4 bytes)**
- **Logical Volume/Data set (4bytes)**
- **Object Offset on the data set (4 bytes)**
- **Object length or displacement identifying a pointer (4 bytes)**

Addressing Space Management

- Mapping of the object names into capabilities managed by system software. Due to the policy/mechanism separation, this mapping may have multiple variations (e.g. the classical Multics/Unix hierarchical style was just a specific case)
- Addressing space of a process defined by its associated set of capabilities
- Dynamic link edit and de-linking
- Virtual address mapping
  - Inefficiency of the "classical" scheme of capability-based architectures (indirection through a Master Object Table)
  - Choice to specialize data sets: data set 0 of logical volume 0 describes the mapping of all logical volumes and data set 0 of each logical volume décribes the mapping of the data sets it contains onto this logical volume
  - Concepts of segment and data set only known at processor level (protection) and memory hierarchy managed in terms of addresses on logical volumes (i.e. levels of intermediate memories are just caches of the latest level)
- Communications based upon the concept of ports

Instruction Set Architecture

- Concept of virtual architectures supported by the common base architecture
- High Level Language machine (HLL Machine) based upon PL/1



Hardware Architecture

- Preliminary studies centered around memory hierarchy (basic hypothesis of the architecture)
- Analysis concerning the choice of the latest level of the memory hierachy (i.e. where the objects reside) e.g. cartridge libraries such as the IBM 3850
- Study of cache coherency protocols in SMP environment. Directory-based protocol patented by L. CENSIER/P. FEAUTRIER
- Architecture simulations not started
- Simplification of process states:
  - Virtually active (i.e. running or waiting for an hardware resource such as processor or a miss in memory hierachy)
  - Waiting for a logical resource

Actors

- Studies of the Y project were software-oriented. Y team under the management of Denis DERVILLE within the System Software Division headed by Claude BOULLE
- Georges LEPICARD, reporting to François SALLE Technical Director, participated to the study
- Architecture leaders: René J CHEVANCE and Jean Louis MANSION
- Software team headed by Jean Louis MANSION: Jean Pierre ARMISEN, Jean Louis DUCHENE, Gérard MION, Michel PONTACQ, Jean Paul RISSEN and Richard WATREMEZ. Claude KAISER: consultant about addressing
- Study of the virtual manachine (HLL Machine) headed by René J CHEVANCE: Gérard BATTAREL and Thierry HEIDET
- Hardware studies: Lucien CENSIER, with Paul FEAUTRIER consultant and participation from Alice RECOQUE
- In the second half of 1974, UNIDATA partners (Philips and Siemens) have been associated to the study

Epilog

- CII and HONEYWELL BULL merge started in 1975, end of UNIDATA
- Two reasons lead the Company to stop the study: convergence between products from CII and HONEYWELL-BULL was top priority on one side and the planned date for Y Line introduction was considered too late on the other side
- Similarities with the architecture of the System/38 (introduced in 1978 and currently known as the AS/400) altough the studies have been conducted in complete isolation
- First experience on capability-based architectures and their implications at system level (consider the ill-fated 432 project from Intel) and on the management of very large addressing spaces